Varactor Frequency Tripler

Nonlinear Microwave Design

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December 12th 2000

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1 Project Goal

Design a Frequency Tripler with:

- → Input Frequency f_{in} = 1 GHz
- → Output Frequency f_{out} = 3 GHz
- → Input / output power ratio (efficiency) as high as possible
- → Power level: somewhere around 10..20dBm, will depend on the device chosen

2 Frequency Multipliers

A frequency multiplier hast the property that the frequency of the output signal has an integer multiple of the input frequency (see Figure 1).

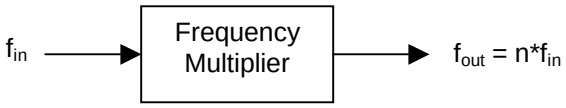


Figure 1 Frequency Multiplier

To obtain a frequency at the output that is an integer multiple of the input frequency we use a nonlinear device. The current dependency (or capacitance dependency) of the device upon the voltage across the device can be written as a Taylor series. Therein we have

$$i = Av + Bv^2 + Cv^3 + \ldots \quad \textbf{(1)}$$

Assuming the input voltage to be a cosine signal, we easily can see that we will get higher order harmonics. This is from the relationships

$$\cos^2 x = \frac{1}{2}\left(1+\cos(2x)\right)$$
$$\cos^3 x = \frac{1}{2}\left(\cos(x)+\cos(x)\cos(2x)\right) = \frac{1}{2}\cos(x)+\frac{1}{4}\left(\cos(x)+\cos(3x)\right) \quad \textbf{(2)}$$
...

Now we want the input signal to enter the circuit and the signal with the output frequency to exit the circuit. Everything else shouldn't be visible from outside. For this reason we not only need a nonlinear device, but also some filters (see Figure 2).

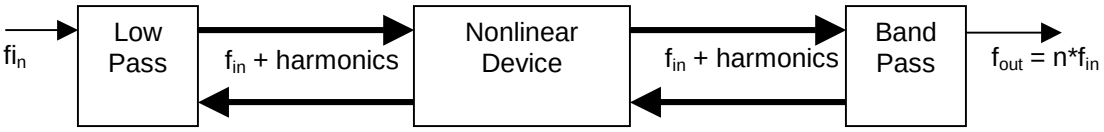


Figure 2 Frequency Multiplier with Filters

From (1) we know that the nonlinear device will produce voltages of higher order from the current of the first harmonic. One of these voltages is of the desired order and will be allowed to exit through the band-pass. How about the other frequencies? Lowpass and bandpass will present a high impedance to all those harmonic voltages, preventing current to flow. Considering that any current in the circuit results in loss (in the parasitic resistances) this is good news. But it turns out that if we allow the currents of the other harmonics to flow, the intermodulation products of those harmonics will contribute to the desired harmonic of the output frequency. Therefore we should try to short the currents of the non-desired harmonics.

As we want to deliver as much power as possible to the circuit and also want to draw as much power as possible from the circuit, the frequency multiplier should be matched at the input (for the input frequency) and at the output (for the output frequency). With these considerations we are left with the block diagram shown in Figure 3.

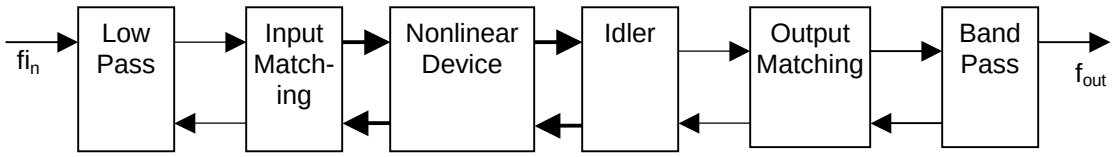


Figure 3 Complete Frequency Multiplier Blockdiagram

To obtain higher order frequency multiplication we can cascade several multipliers. This can increase conversion efficiency but also increases complexity.

There are different possibilities concerning the nonlinear device. We need a device with a nonlinear characteristic in order to produce higher order harmonics. This nonlinear characteristic might be a nonlinear I/V or C/V relationship. As we want to design a frequency multiplier with high efficiency, and not high bandwidth, we prefer the nonlinear C/V characteristic. A Varactor diode is such a device.

3 Varactor Frequency Multiplier

Varactor diode frequency multipliers in general generate very little noise (phase- as well as amplitude-noise). The only noise source is the thermal noise of the series resistance of the Varactor and the circuit loss resistances.

If we are using Schottky-barrier varactor diodes we can obtain output frequencies of up to several hundred giga-hertz.

The varactor always has a parasitic resistance in series, which dissipates power. In order to minimize the loss power, one would tend to present an open for all the undesired harmonics, resulting in zero current and therefore no loss. At the example of the pure square-law diode we see that it produces only a second order harmonic directly. Is a current at the second harmonic prohibited, we don't get the desired higher order harmonics. If current is allowed at the 2^{nd} harmonic, it will mix with the first harmonic and generate therefore higher order harmonics. This is the reason to present a short to the undesired (intermediate) harmonics. The shorting circuits are called idlers.

As the varactor is a high Q device and the idlers also should have a high Q we get a very narrow banded circuit. Therefore varactor multipliers have a very narrow bandwidth.

3.1 Design procedure

- → Find a varactor diode appropriate for the desired frequency and power level.
- → Determine the parameters of the diode (fitting factor γ, diffusion potential ϕ, zero bias junction capacitance C_{j0}, reverse breakdown voltage V_b, and series resistance R_s).
- → Find the source, load and idler impedances of the diode.
- → Design matching circuits and idler resonators.

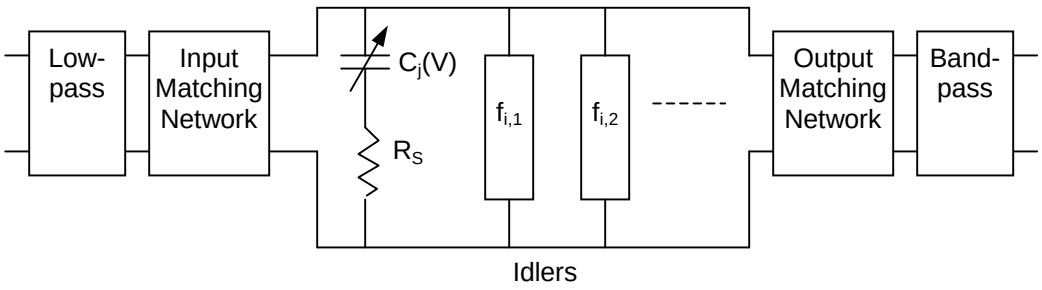


Figure 4 Varactor frequency multiplier, biasing circuit not shown

3.2 Analysis

This analysis was extracted from [2]. From [1] we have the relation

$$C(V) = \frac{dQ(V)}{dV} = \frac{C_{j0}}{\left(1 - \frac{V}{\phi}\right)^{\gamma}} \tag{3}$$

therefore

$$Q(V) = \int C(V)dV = \frac{C_{j0} \cdot \phi}{\gamma - 1} \cdot \left(1 - \frac{V}{\phi}\right)^{1-\gamma} \tag{4}$$

or

$$V(Q) = \phi \cdot \left[1 - \left(-\frac{Q \cdot (\gamma - 1)}{C_{j0} \cdot \phi}\right)^{\frac{1}{1-\gamma}}\right] \tag{5}$$

Looking at the representation of the varactor diode in Figure 5

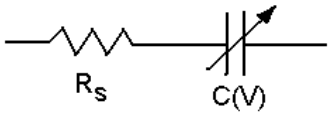


Figure 5 Varactor equivalent circuit

we can write the voltage v_j across the nonlinear capacitor as a function of the charge Q on the nonlinear capacitor.

$$\frac{v_j - \phi}{V_B - \phi} = f\left(\frac{Q - Q_\phi}{Q_B - Q_\phi}\right) \tag{6}$$

Where:

- vj: voltage across capacitor
- ϕ: diffusion potential
- V_B: reverse breakdown voltage
- Q: charge on capacitor
- Q_ϕ: charge on capacitor at voltage ϕ
- Q_B: charge on capacitor at voltage V_B

Or we can write

$$\varphi = f(q) \tag{7}$$

Where:

φ: normalized voltage across capacitor

q: normalized charge on capacitor

With

$$\begin{aligned} v_j &= (V_B - \phi)\cdot f(q) + \phi \\ i &= \frac{dQ}{dt} = \frac{dq}{dt}\cdot (Q_B - Q_\phi) \end{aligned} \tag{8}$$

we can write the total voltage across the varactor as

$$V_{tot} = v_j + R_S \cdot i = (V_B - \phi)\cdot f(q) + \phi + R_S \cdot (Q_B - Q_\phi)\frac{dq}{dt} \tag{9}$$

Now φ, q and i can be expressed as Fourier series

$$\begin{aligned} \varphi &= \sum_{-\infty}^{\infty} \varphi_k \cdot e^{jk\omega_0 t} \\ q &= \sum q_k \cdot e^{jk\omega_0 t} \\ \frac{dq}{dt} &= \sum I_k \cdot e^{jk\omega_0 t} = \sum jk\omega_0 q_k \cdot e^{jk\omega_0 t} \end{aligned} \tag{10}$$

The sum for q and dq/dt has to be taken over all harmonics k at which current is flowing. This is defined by the actual circuit.

In order to find the input, output and idler impedances we need to find φ_k and q_k. These values we can not get analytically, but need to find them numerically. In [2] the following procedure is suggested:

- → Apply an input current.
- → Get the voltages across the diode due to the current from it's Q/V relationship.
- → Calculate new currents from these voltages.
- → Get the voltages across the diode due to the currents from it's Q/V relationship
- → … and so on, until the currents reach their asymptotic values.

Other methods are available in [3]. We will use an own approach, outlined in 3.4.

3.2.1 Load Impedance

For the voltage V_l at the load port and at the frequency f=l*ω_0 we get

$$V_l = (V_B - \phi)\varphi_l + R_S \cdot (Q_B - Q_\phi) \cdot I_l = -Z_l \cdot (Q_B - Q_\phi) \cdot I_l \quad \textbf{(11)}$$

or with

$$\kappa = \frac{V_B - \phi}{(Q_B - Q_\phi) \cdot R_S} \quad \textbf{(12)}$$

we can write

$$-\frac{Z_l}{R_S} = \kappa \cdot \frac{\varphi_l}{j\omega_0 l q_l} + 1 \quad \textbf{(13)}$$

where l is the integer factor between the fundamental (input frequency) and the harmonic (output frequency) at the load.

3.2.2 Idler Impedance

With essentially the same derivation as for the load impedance we get

$$-\frac{Z_i}{R_S} = \kappa \cdot \frac{\varphi_i}{j\omega_0 i q_i} + 1 \quad \textbf{(14)}$$

3.2.3 Input Impedance

$$Z_{in} = \frac{inp.voltage}{inp.current}$$

$$Z_{in} = \frac{(V_B - \phi) \cdot \varphi_{in}}{I_{in} \cdot (Q_B - Q_\phi)} + R_S \quad \textbf{(15)}$$

$$\frac{Z_{in}}{R_S} = \kappa \cdot \frac{\varphi_{in}}{j\omega_0 q_{in}} + 1$$

3.3 Finding a Varactor device

Varcator diodes can come in the following types:

- → Schottky-barrier varactor diodes
- → Step recovery diodes
- → p+n (diffused epitaxial varactor) diodes in Silicon or GaAs

Not suitable are:

- → Hyperabrupt diodes due to their high series resistance
- → Mixer diodes, as those are optimized for their nonlinear I/V characteristic and low capacitance.

As we only want to design a frequency tripler, we do not need to use a step recovery diode, which generates a very high range of harmonics.

Now we are left with Schottky-barrier varactor diodes and the p^+n diodes. So let's compare the properties:

Schottky-barrier varactor diode

- → Typically lower series resistance
- → Good for very high frequencies

p^+n diode

- → Increased capacitance variation due to effect of minority carrier charge storage.
- → Due to the larger capacitance variation we get a higher power handling capacity.
- → Useful only for lower frequencies (<20..40 GHz).

A figure of merit is the dynamic cutoff frequency f_{cd}.

$$f_{cd} = \frac{S_{max} - S_{min}}{2 \cdot \pi \cdot R_S} \approx \frac{S_{max}}{2 \cdot \pi \cdot R_S} \qquad \textbf{(16)}$$

Where S is the elastance or inverse capacitance. As S_{min} (elastance as ϕ is approached) is very small it often can be neglected. We should operate the diode well below f_{cd}.

The parameters of the diode we need to know for our design are:

- → The diffusion potential ϕ (a typical value for Schottky-barrier varactor diodes is 1 V)
- → γ, normally around 0.5

- → The zero bias junction capacitance C_{j0}
- → The reverse breakdown voltage V_b
- → The series resistance R_S

We can calculate the nonlinear capacitance as:

$$C(V) = \frac{C_{j0}}{\left(1 - \frac{V}{\phi}\right)^{\gamma}} \tag{17}$$

As we want to design a circuit and want to be able to simulate it, we try to find a suitable varactor diode among the RF-diode models provided with ADS. Looking at the list of RF-diode models in ADS we find diodes for mixing, switching, clamping, tuning and general purposes. For our frequency multiplier we are interested in varactors. Varactors are also used for tuning. So we should look for the models that are marked for tuning purposes.

Looking at these diodes we are looking for one for which we get a data sheet and the necessary parameters (again, this is just for practical reasons).

Table 1 Varactor diodes with models in ADS

Manufacturer	Model	C1	C2	RS
Hitachi	HVU202A	15.2pF @V_R=2V	2.15pF @V_R=25V	0.57Ω @V_R=5V, f=470MHz
	HVU306A	32pF @V_R=2V	2.75pF @V_R=25V	0.75Ω @V_R=5V, f=470MHz
Philips	BBY31 [1)]	16.5pF @V_R=1V	1.8pF @V_R=28V	max 1.2Ω @f=470MHz, C_d=9pF
Siemens	BBY… [1)]			
	BB535	15pF @V_R=2V	2.24pF @V_R=25V	0.55Ω @V_R=3V, f=470 MHz
	BB639	29.75pF @V_R=2V	2.85pF @V_R=25V	0.65Ω @C_T=12pF, f=100 MHz
	BB640	54.5pF @V_R=2V	3.28pF @V_R=25V	1.15Ω @C_T=12pF, f=100 MHz
	BB831	8.8pF @V_R=1V	1.02pF @V_R=28V	1Ω @V_R=1V, f=100 MHz
	BB833	9.3pF @V_R=1V	0.75pF @V_R=28V	1.8Ω @V_R=1V, f=100 MHz
Toshiba	1SV214	15pF @V_R=2V	2.3pF @V_R=25V	0.4Ω @V_R=5V, f=470 MHz
	1SV215	29pF @V_R=2V	2.8pF @V_R=25V	0.6Ω @V_R=5V, f=470 MHz

1) From the Siemens Homepage we see that diodes with the name BBY… are hyperabrupt diodes, which are not suitable for our purpose (R_S is too high).

→ The Motorola models included in ADS are no good, as Motorola went out of business with discrete semiconductors several years ago. Crystalonics is producing a variety of these diodes now, but doesn't provide any data sheets on the Internet.

→ Sony discontinued the Sony diode models included in ADS.

In general Siemens provides the most data with its diodes. Therefore a Siemens diode would be preferable. Other possibilities are Toshiba or Hitachi.

3.3.1 Siemens BB535

Let's have a closer look at the Siemens BB535 [4]. With a series resistance of 0.55 Ω and a minimal capacitance of 2.24 pF we get a dynamic Q of Q_δ=129, which is good. The dynamic cutoff frequency is f_{cd}=122 GHz. Even though the data sheet gives little information on the device parameters we can find Spice parameters on the Siemens Homepage [5]. These Parameters are given separately for the diode chip and the package. One has to find out what the different Spice parameters represent and combine the data of the package and the chip to obtain the necessary data.

The BB535 is packed in a SOD-323 package. The equivalent circuit for the package is shown in Figure 6.

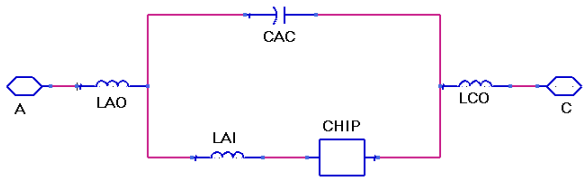


Figure 6 SOD323 package equivalent circuit

The parameters are:

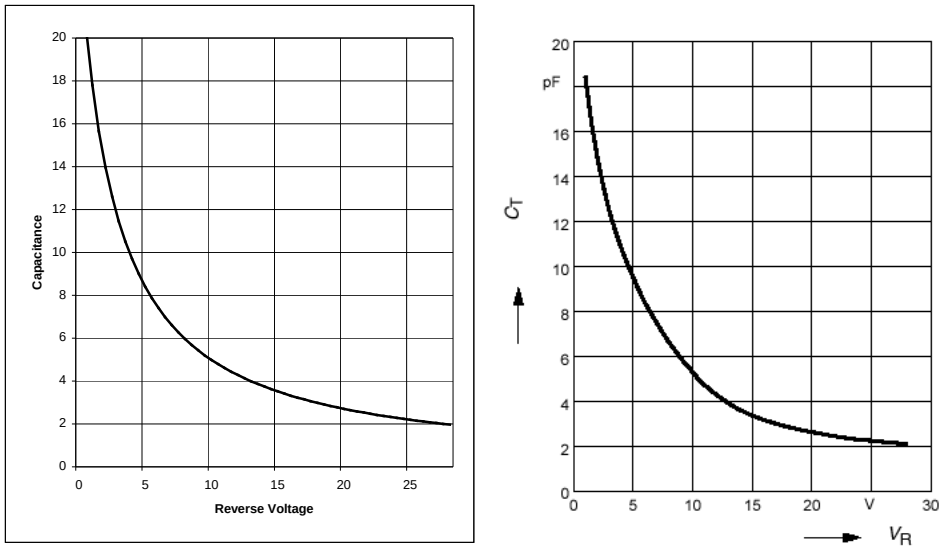
LAI = 0.55 nH
CAC = 0.11 pF
LAO = 0.67 nH
LCO = 0.55 nH

The Spice model parameters for the chip are:

IS=2.276E-15
N=1.063
RS=0.2099
XTI=3
EG=1.11
CJO=24.4E-12
M=1.064
VJ=2.90
FC=0.5
BV=32

IBV=100E-9
TT=120E-9

We can identify R_S as the ohmic series resistance. C_{j0} is the zero bias capacitance. V_J is the diffusion potential ϕ and M is the fitting exponent γ. To verify the correctness of this assumption, we generate a plot using these parameters in (17). In Figure 7 we can see that the curves fit approximately. So we conclude that we can represent this diode with (17) and the parameters C_{j0} = 24.4 pF, ϕ = 2.9 V and γ = 1.064.



(a) (b)

Figure 7 (a) Calculated capacitance and (b) given curve in data sheet

3.4 Practical Approach with ADS

As the method outlined in 3.2 does involve lots of programming, we try to use available computer software to solve the problem. Looking at Figure 4 we can see that, due to the filters, a current with the fundamental frequency flows only through the input circuit. A current of the second harmonic flows only through the idler circuit. Finally, a current of the third harmonic flows only through the output circuit. This assumption, of course, is only valid for an ideal circuit with ideal filters. In reality the three circuits (input, idler, output) are not strictly separated. For the analysis we treat them as if completely separated and compensate in the design for the non-ideal circuits. We now represent the ideal circuits, seen by the diode, as current sources of the respective frequencies.

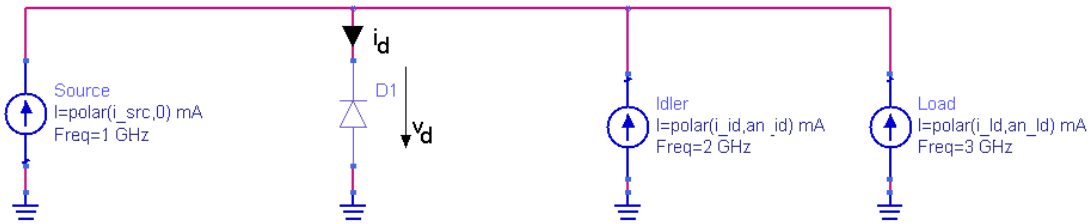


Figure 8 Simplified circuit, shown without biasing circuit

In all the following steps we do not mention the bias voltage but understand that it needs to be adjusted, so that there is no dc current flowing through the diode. We now apply a current of the fundamental frequency. We adjust the idler and output current and phase to maximize the real power dissipated in the load (current source). Thereby the phasor diagrams shown in Figure 9 and Figure 13 from [2] are of great help.

The real power from a source or delivered is calculated by

$$P_i = real(V_i \cdot I_i^*) \tag{18}$$

Using the voltage components across the diode V_i and the current components through the diode I_i, where the index i denotes the number of the harmonic (i.e. source=1, idler=2, load=3) we get a positive value for power delivered to the diode (i.e. source) and negative values for power delivered by the diode (i.e. load). The power delivered to the idler circuit ideally should be zero. As the two current sources at the idler and load frequencies actually represent passive circuits, the power at these frequencies must be negative or zero.

$$P_{id}, P_{ld} = P_2, P_3 \leq 0 \tag{19}$$

Now we apply this method to our design. First we let only a source current flow through the diode and look at the voltages. As shown in Figure 9 we gat a voltage at the fundamental (or first harmonic), which lags the current by 90°, which we of course expect for a capacitive load (varactor). The voltage of the second harmonic lags another 90° and the third again another 90°.

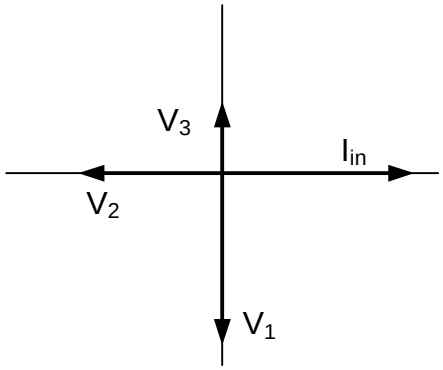


Figure 9 Phasor diagram of the voltages across the unloaded varactor diode

3.4.1 Optimization Circuit

Now we set up an ADS simulation in order to optimize the free parameters. Those are the three currents, the phases of the idler and load currents and also the bias voltage (see Figure 10).

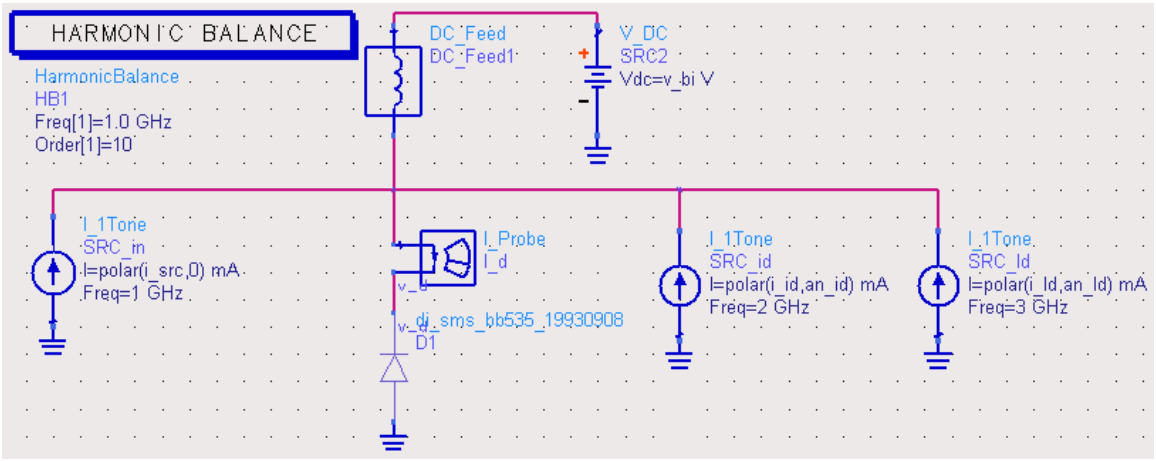


Figure 10 Circuit in ADS for optimization

In order to get a good result from an optimization we need to things. Those are good optimization goals and a start value close to the optimum result.

3.4.2 Optimization Goals

Let's have a look at the optimization goals. First we define the value 'Pow' (see Figure 11 (a)). It is a vector with the real powers at each harmonic. For example 'Pow[1]' represents the real power at the first harmonic. Again, this power is positive if power is delivered to the diode and negative if power is delivered by the diode. This comes from the definition of the current through the diode.

Now we want a maximum efficiency. This we can express by maximizing the negative ratio of the real power at the third harmonic over the real power at the first harmonic (see Figure 11 (b)). Once again, negative because the real power at the third harmonic is negative and the one at the first harmonic positive. We want to make sure that the circuit works as frequency tripler, or, in other words consumes power at the first harmonic and gives power at the third harmonic and not the other way round. Therefore we demand the input power to be greater than zero (see Figure 11 (c)). Here we also can define an upper limit of input power. Finally we want to make sure that the idler circuit is passive, i.e. real power at the second harmonic is zero or less (see Figure 11 (d)).

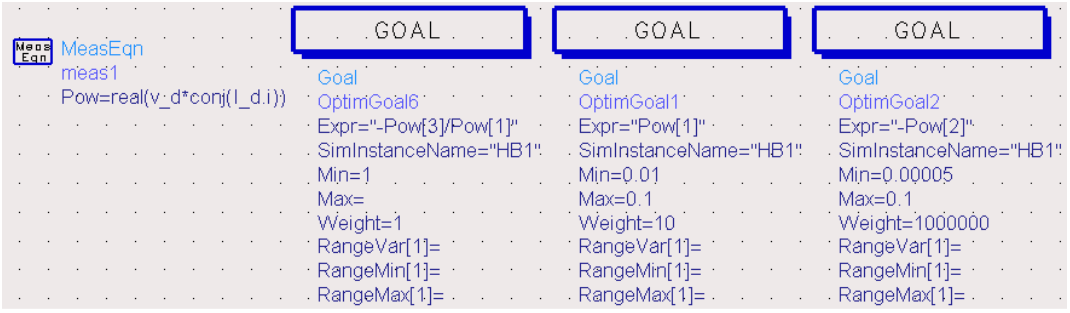


Figure 11 Set of optimization goals

3.4.3 Optimization Start Values

With the optimization goals we have accurately defined what we want. Now we have to obtain good start values for the optimization parameters. Looking again at the phasor diagram of the voltage components across the unloaded diode in Figure 9 we can estimate the angles of the idler and load current. First, as the phasor diagram is for the unloaded diode, we set the currents at second and third harmonic to very small values. The phase of the idler current we set to –90°. Finally we set the phase of load current to 180°.

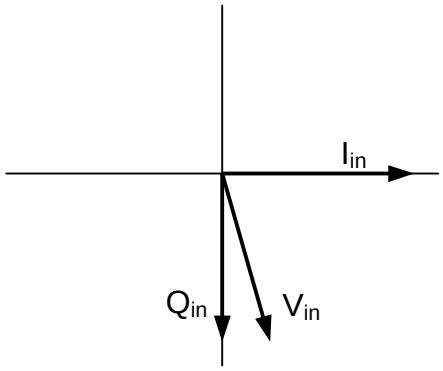


Figure 12 Expected phasor diagram of the input values

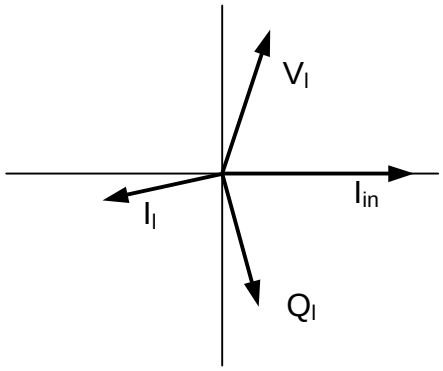


Figure 13 Expected phasor diagram of the output values

3.4.4 ADS optimization

Using the above goals and start values we run an ADS optimization for that circuit. We expect the optimization to increase the idler and load currents in order to fulfill the input power and efficiency goals. While increasing the currents the angles will be corrected to satisfy the goals. Using this optimization we get the following results:

Efficiency:	0.876
Bias Voltage:	6.46V
Input Power:	94mW = 19.7dBm
Output Power:	83mW = 19.2dBm
Loss Power:	11mW = 10.4dBm
Input Impedance:	(1.09-j9.99)Ω
Idler Impedance:	-j6.96Ω
Output Impedance:	(6.00-j30.46)Ω

3.5 Design

Now we try to design a circuit fulfilling the requirements obtained from the optimization. Figure 14 Shows the circuit used for this purpose. We know the required input impedances of the lowpass and bandpass filter. We also know the impedance of the idler circuit. All the impedances are fairly low, so we can design the three circuits separately by implying the restriction that the circuit has to present a high impedance at the other two frequencies. With high impedance we think of something around 200Ω.

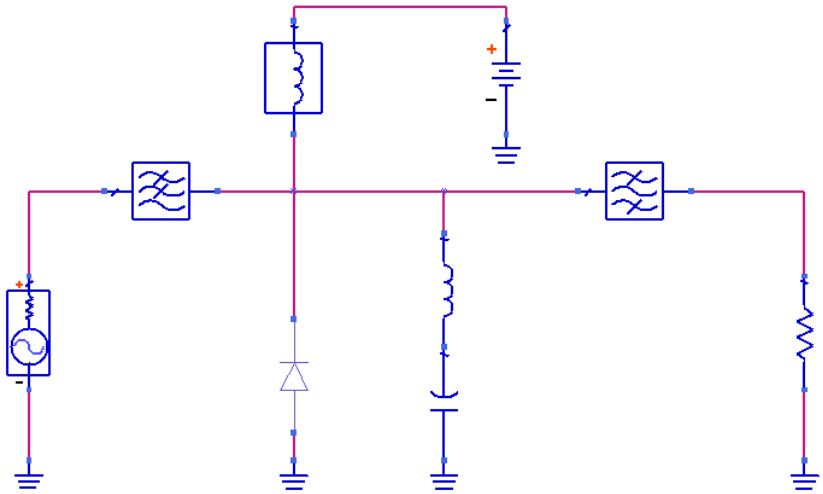


Figure 14 Frequency tripler circuit

We need an idler circuit presenting –j6.9Ω at 2GHz and at least ±j200Ω at 3 respectively 1GHz. Using a series LC resonator we get the design equations

$$\begin{aligned} j2\omega_0 L + \frac{1}{j2\omega_0 C} &= -j6.96 \\ j3\omega_0 L + \frac{1}{j3\omega_0 C} &= j200 \end{aligned} \qquad \textbf{(20)}$$

From this we get the values for the inductor and capacitor of the idler circuit.

$$\begin{aligned} C &= 0.35\,pF \\ L &= 17.5nH \end{aligned} \qquad \textbf{(21)}$$

Figure 15 shows the smith chart of the idler circuit.

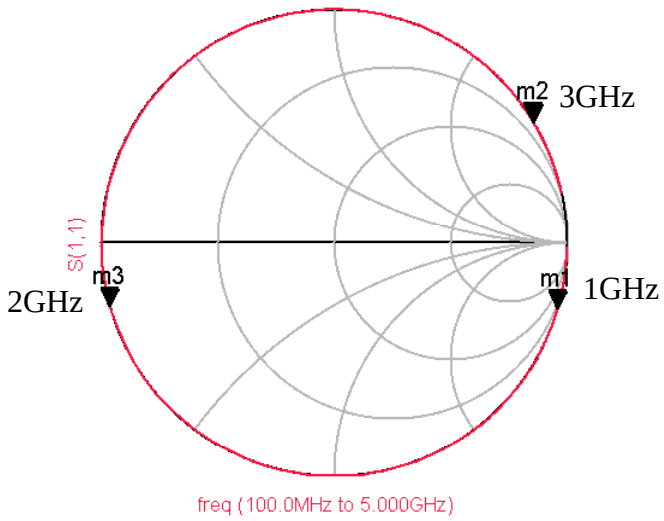


Figure 15 Smith chart of the idler circuit

Now we are left with designing the matched low and bandpass filter. Unfortunately we do not have any more time to actually design these circuits. Also we cannot use the ADS filter blocks, as those only allow real input impedances. One could use the filter blocks plus matching networks. This attempt failed as the harmonic balance simulation always terminated in an error (No unique solution for the circuit). So one is left with designing matched filters, which present a high enough impedance at the other two frequencies.

4 Conclusions

Varactor multipliers, compared to the varistor multipliers, are very complex to handle. One really has to have a need for the advantages of the varactor multiplier to use it.

Using the approach outlined in 3.4 requires no programming and can save time. But as we couldn't show a complete example it is not proven that this method works all through the design.

As we deal here with a nonlinear device and use numerical methods to find a solution, we don't get one optimum solution. Every time an optimization is performed, the software is coming up with a different, sometimes similar solution. Programming own software solving for a solution would have the advantage that one can investigate into intermediate results of the optimization to understand what the solution really represents.

This project, though time consuming and not really brought to completion, was very helpful in understanding the principles and methods when dealing with nonlinear circuits.

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